



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,514	03/09/2004	John P. Snyder	14467.05	1961
25763	7590	05/20/2005	EXAMINER	
DORSEY & WHITNEY LLP INTELLECTUAL PROPERTY DEPARTMENT 50 SOUTH SIXTH STREET MINNEAPOLIS, MN 55402-1498			KIM, SU C	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/796,514

Applicant(s)

SNYDER ET AL.

Examiner

Su C. Kim

Art Unit

2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 09 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-96 is/are pending in the application.
- 4a) Of the above claim(s) 66-96 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-65 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to..
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 March 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 11/22/04
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## REMARKS/ARGUMENTS

Applicant has canceled claims 66-96. Claims 66-96 have been withdrawn from consideration.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 1, 3-9, 15, 17-24, 26-36, 38-47, 49-58, and 60-65 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuo et al (US 6737716 B1)

providing for a semiconductor substrate **300**; providing for an electrically insulating layer **309, 313, & 314** in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0 (**Column 16, lines 4-9, please note that Matsuo teaches that insulating films or gate insulating films can be formed with metal oxide films and also specifies elements such as titanium**

Art Unit: 2823

**oxide, zirconium oxide, hafnium oxide, tantalum oxide, niobium oxide, aluminum oxide, cerium oxide, yttrium oxide or yttrium-zirconium oxide. Some of those metal oxides have high dielectric constant: hafnium oxide (~30), titanium oxide (50-60), titanium oxide (40-50), Zirconium Oxide (12.5), tantalum oxide (11.6) and .etc according to dielectric constant index);**

providing for a gate electrode **312 & 310** in contact with at least a portion of the insulating layer **313 & 314**;

and providing a source electrode and a drain electrode **305, 307, & 317** in contact with the semiconductor substrate **300** and proximal to the gate electrode **312 & 310** wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate (**column 6, lines 19-59, see more details in the manufacturing method H**).

3. With respect claim 3, Matsuo discloses, the method of claim 1, wherein the source and drain electrodes **305, 307, & 317** are formed from a member of the group consisting of the rare earth silicides (**column 11, lines 25-40, please note yttrium and cerium are rare earth materials**).

Art Unit: 2823

4. With respect claim 4, Matsuo discloses, the method of claim 1, wherein the insulating layer **309, 313, & 314** is formed from a member of the group consisting of metal oxides **313 & 314 (column 34, lines 25-27)**.

5. With respect claim 5, Matsuo discloses, the method of claim 1, wherein the insulating layer **309, 313, & 314** is formed from an oxy-nitride stack **314**. **(Column 10, lines 52-67 & column 11, lines 1-30 Please note that applicant defines oxy-nitride stack as “unary oxide such as Ta<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, ZrO<sub>2</sub>, HfO<sub>2</sub>, Y<sub>2</sub>O<sub>3</sub>, La<sub>2</sub>O<sub>3</sub>, Gd<sub>2</sub>O<sub>3</sub>, Sc<sub>2</sub>O<sub>3</sub> or silicates ZrSiO<sub>4</sub>, HfSiO<sub>4</sub>, LaSiO<sub>4</sub>, TiSiO<sub>4</sub>”).**

6. With respect claim 6, Matsuo discloses, the method of claim 1, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel **(column 6, lines 33-35)**.

7. With respect claim 7, Matsuo discloses, the method of claim 1, wherein an entire interface between at least one of the source electrode and the drain electrode **305, 307, & 317** and the semiconductor substrate **300** forms a Schottky contact or Schottky-like region with the semiconductor substrate **(column 6, lines 19-59, see more details in the manufacturing method H)**.

8. With respect claim 8, Matsuo discloses, the method of claim 1, wherein dopants **305** are introduced into the channel region **(column 31, lines 14-16)**.

9. With respect claim 9, Matsuo discloses, the method of claim 1, wherein the insulating layer includes more than one layer **309, 313, & 314**.

10. With respect to claim 12, the method of claim 10, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel, and wherein dopants **305** are introduced into the channel region. **(Column 6, lines 19-59 & column 31, lines 14-16, see more details in the manufacturing method H).**

11. With respect to claim 15, Matsuo discloses a method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate **300**; providing for an electrically insulating layer **309, 313, & 314** in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 7.6 **(See detail of rejections on claim 1, please note hafnium oxide has greater a dielectric constant (~30) than claim 15 as defined);**

providing for a gate electrode **312 & 310** in contact with at least a portion of the insulating layer **309, 313, & 314**;

and providing a source electrode and a drain electrode **305, 307, & 317** in contact with the semiconductor substrate **300** and proximal to the gate electrode **312 & 310** wherein at least one of the source electrode and the drain electrode **305, 307, & 317** forms a Schottky contact or Schottky-like region with the semiconductor substrate **(column 6, lines 19-59, see more details in the manufacturing method H)**.

12. With respect to claim 17, Matsuo discloses, the method of claim 15, wherein the source and drain electrodes **305, 307, & 317** are formed from a member of the group consisting of the rare earth silicides **(column 11, lines 25-40, please note yttrium and cerium are rare earth materials)**.

13. With respect to claim 18, Matsuo discloses, the method of claim 15, wherein the insulating layer **309, 313, & 314** is formed from a member of the group consisting of metal oxides **313 & 314 (Column 32, line 17)**.

14. With respect to claim 19, Matsuo discloses, the method of claim 15, wherein the insulating layer is formed from an oxy-nitride stack **314. (Column 10, lines 52-67 & column 11, lines 1-30 Please note applicant defines oxy-nitride stack as “unary oxide such as Ta<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, ZrO<sub>2</sub>, HfO<sub>2</sub>, Y<sub>2</sub>O<sub>3</sub>, La<sub>2</sub>O<sub>3</sub>, Gd<sub>2</sub>O<sub>3</sub>, Sc<sub>2</sub>O<sub>3</sub> or silicates ZrSiO<sub>4</sub>, HfSiO<sub>4</sub>, LaSiO<sub>4</sub>, TiSiO<sub>4</sub>”)**.

Art Unit: 2823

15. With respect to claim 20, Matsuo discloses, the method of claim 15, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel (**column 6, lines 19-59, see more details in the manufacturing method H**).

16. With respect to claim 21, Matsuo discloses, the method of claim 15, wherein an entire interface between at least one of the source electrode and the drain electrode **305, 307, & 317** and the semiconductor substrate **300** forms a Schottky contact or Schottky-like region with the semiconductor substrate (**column 6, lines 19-59, see more details in the manufacturing method H**).

17. With respect to claim 22, Matsuo discloses, the method of claim 15, wherein the insulating layer includes more than one layer **309, 313, & 314**.

18. With respect to 23, Matsuo discloses, the method of claim 15, wherein dopants **305** are introduced into the channel region (**column 31, lines 14-16**).

19. With respect to claim 24, Matsuo discloses a method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate **300**; providing for an electrically insulating layer **309, 313, & 314** in contact with the semiconductor substrate, the

Art Unit: 2823

insulating layer having a dielectric constant greater than 15 (**See more details of rejection on claim 1, please note Hafnium oxide has greater dielectric constant (~30) than claim 24 as defined**);

providing for a gate electrode **312 & 310** in contact with at least a portion of the insulating layer **313 & 314**; and

20. providing a source electrode and a drain electrode **305, 307, & 317** in contact with the semiconductor substrate **300** and proximal to the gate electrode **312 & 310** wherein at least one of the source electrode and the drain electrode forms a Schottky contact or Schottky-like region with the semiconductor substrate (**column 6, lines 19-59, see more details in the manufacturing method H**).

21. With respect claim 26, Matsuo discloses, the method of claim 24, wherein the source and drain electrodes **305, 307, & 317** are formed from a member of the group consisting of the rare earth silicides (**column 11, lines 25-40, please note yttrium and cerium are rare earth materials**).

22. With respect to claim 27, Matsuo discloses, the method of claim 24, wherein the insulating layer is formed from a member of the group consisting of metal oxides **313 & 314** (**column 34, lines 25-27**).

Art Unit: 2823

23. With respect to claim 28, Matsuo discloses, the method of claim 24, wherein the insulating layer **309, 313, & 314** is formed from an oxy-nitride stack **314**. **(Column 10, lines 52-67 & column 11, lines 1-30 Please that applicant defines oxy-nitride stack as “unary oxide such as Ta<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, ZrO<sub>2</sub>, HfO<sub>2</sub>, Y<sub>2</sub>O<sub>3</sub>, La<sub>2</sub>O<sub>3</sub>, Gd<sub>2</sub>O<sub>3</sub>, Sc<sub>2</sub>O<sub>3</sub> or silicates ZrSiO<sub>4</sub>, HfSiO<sub>4</sub>, LaSiO<sub>4</sub>, TiSiO<sub>4</sub>”).**

24. With respect to claim 29, Matsuo discloses, the method of claim 24, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel **(column 6, lines 19-59, see more details in the manufacturing method H).**

25. With respect to claim 30, Matsuo discloses, the method of claim 24, wherein an entire interface between at least one of the source electrode and the drain electrode **305, 307, & 317** and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate **300 (column 6, lines 19-59, see more details in the manufacturing method H).**

26. With respect to claim 31, Matsuo discloses, the method of claim 24, wherein dopants **305 & 307** are introduced into the channel region **(column 31, lines 14-16).**

27. With respect to claim 29, Matsuo discloses, the method of claim 24, wherein the insulating layer includes more than one layer **309, 313, & 314.**

Art Unit: 2823

28. With respect to claim 33, Matsuo discloses a method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate **300**;

providing for an electrically insulating layer in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than 4.0(**See more detail of rejection on claim 1, please note hafnium oxide has greater dielectric constant (~30) than claim 33 as defined**);

providing for a gate electrode **312 & 310** located in contact with at least a portion of the insulating layer **313 & 314**; exposing the semiconductor substrate on one or more areas proximal to the gate electrode (**column 6, line 19-37, please see details in the manufacturing method H**);

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate(**column 6 , lines 33-35**);

29. and reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate **300** (**column 6, lines 19-59, see more details in the manufacturing method H**).

30. With respect to claim 34, Matsuo discloses the method of claim 33, wherein the gate electrode **312 & 310** is provided by:

depositing a thin conducting film **311** on the insulating layer **302 (please note polysilicon is a conducting film)**;

patterning and etching the conducting film **311** to form a gate electrode **312 & 310**;

and forming one or more thin insulating layers **309 & 314** on one or more sidewalls of the gate electrode **312 & 310**.

31. With respect to claim 35, Matsuo discloses the method of claim 33, further comprising removing metal not reacted during the reacting process (**column 32, line 50**).

32. With respect to claim 36, Matsuo discloses the method of claim 33, wherein the reacting comprises thermal annealing (**column 32, line 35-36**).

33. With respect to claim 38 Matsuo discloses the method of claim 33, wherein the source and drain electrodes are formed from a member of the group consisting of the

Art Unit: 2823

rare earth silicides (column 11, lines 25-40, please note yttrium and cerium are rare earth materials).

34. With respect to claim 39, Matsuo discloses the method of claim 33, wherein the insulating layer 309, 313, & 314 is formed from a member of the group consisting of metal oxides 317(column 34, lines 25-27).

35. With respect to claim 40, Matsuo discloses the method of claim 33, wherein the insulating layer 309, 313, & 314 is formed from an oxy-nitride stack 314. (Column 10, lines 52-67 & column 11, lines 1-30 Please note applicant defines oxy-nitride stack as “unary oxide such as Ta<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, ZrO<sub>2</sub>, HfO<sub>2</sub>, Y<sub>2</sub>O<sub>3</sub>, La<sub>2</sub>O<sub>3</sub>, Gd<sub>2</sub>O<sub>3</sub>, Sc<sub>2</sub>O<sub>3</sub> or silicates ZrSiO<sub>4</sub>, HfSiO<sub>4</sub>, LaSiO<sub>4</sub>, TiSiO<sub>4</sub>”)

36. With respect to claim 41, Matsuo discloses the method of claim 33, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel (column 6, lines 19-53, see more details in the manufacturing method H).

37. With respect to claim 42, Matsuo discloses the method of claim 33, wherein an entire interface between at least one of the source electrode and the drain electrode and the semiconductor substrate forms a Schottky contact or Schottky-like region with

Art Unit: 2823

the semiconductor substrate **300** (column 6, lines 19-59, see more details in the manufacturing method H).

38. With respect to claim 43, Matsuo discloses the method of claim 33, wherein dopants **305** are introduced into the channel region.

39. With respect to claim 44, Matsuo discloses a method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate **300**;

providing for an electrically insulating layer **309, 313, & 314** in contact with the semiconductor substrate **300**, the insulating layer having a dielectric constant greater than 7.6 (See more details on rejected claim 1, please note hafnium oxide has greater a dielectric constant (~30) than claim 33 as defined);

providing for a gate electrode **312 & 310** located in contact with at least a portion of the insulating layer **313, & 314**;

exposing the semiconductor substrate on one or more areas proximal to the gate electrode **312 & 310** (column 6, lines 19-37, Please see details in the manufacturing method H );

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate **(column 6, line 33)**;

and reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate **300 (column 6, lines 19-53, see more details in the manufacturing method H)**.

40. With respect to claim 45, Matsuo disclose the method of claim 44, wherein the gate electrode **310 & 312** is provided by:

depositing a thin conducting film **311** on the insulating layer **309, 313, & 314**;

patterning and etching the conducting film **311** to form a gate electrode **312**;

and forming one or more thin insulating layers **309, & 314** on one or more sidewalls of the gate electrode **312 & 310**.

41. With respect to claim 46, Matsuo discloses the method of claim 44, further comprising removing metal not reacted during the reacting process **(column 6, lines 37-39 see more details in the manufacturing method H)**.

42. With respect to claim 47, Matsuo discloses the method of claim 44, wherein the reacting comprises thermal annealing (**column 6, lines 35, see more details in the manufacturing method H**).

43. With respect to claim 49, Matsuo discloses the method of claim 44, wherein the source and drain electrodes **305, 307, & 317** are formed from a member of the group consisting of the rare earth silicides (**column 11, lines 25-40, please note yttrium and cerium are rare earth materials**).

44. With respect to claim 50, Matsuo discloses the method of claim 44, wherein the insulating layer **309, 313, & 314** is formed from a member of the group consisting of metal oxides **313 & 314 (column 34, lines 25-27)**.

45. With respect to claim 51, Matsuo discloses the method of claim 44, wherein the insulating layer **309, 313, & 314** is formed from an oxy-nitride stack **314**. (**Column 10, lines 52-67 & column 11, lines 1-30 Please note applicant defines oxy-nitride stack as “unary oxide such as Ta<sub>2</sub>O<sub>3</sub>, TiO<sub>2</sub>, ZrO<sub>2</sub>, HfO<sub>2</sub>, Y<sub>2</sub>O<sub>3</sub>, La<sub>2</sub>O<sub>3</sub>, Gd<sub>2</sub>O<sub>3</sub>, Sc<sub>2</sub>O<sub>3</sub> or silicates ZrSiO<sub>4</sub>, HfSiO<sub>4</sub>, LaSiO<sub>4</sub>, TiSiO<sub>4</sub>”**).

Art Unit: 2823

46. With respect to claim 52, Matsuo discloses the method of claim 44, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel (**column 6, lines 19-53, see more details in the manufacturing method H**).

47. With respect to claim 53, Matsuo discloses the method of claim 44, wherein an entire interface between at least one of the source electrode and the drain electrode **305, 307, & 317** and the semiconductor substrate forms a Schottky contact or Schottky-like region with the semiconductor substrate **300** (**column 6, lines 19-53, see more details in the manufacturing method H**).

48. With respect to claim 54, Matsuo discloses the method of claim 44, wherein dopants **305** are introduced into the channel region (**column 31 lines 14-16**).

49. With respect to claim 55, Matsuo discloses a method for manufacture of a device for regulating the flow of electrical current, the method comprising:

providing for a semiconductor substrate **300**;

providing for an electrically insulating layer **309, 313, & 314** in contact with the semiconductor substrate, the insulating layer having a dielectric constant greater than **15** (**See more details of rejections on claim 1, please note hafnium oxide has greater a dielectric constant (~30) than claim 33 as defined**);

providing for a gate electrode **312 & 310** located in contact with at least a portion of the insulating layer **313 & 314**;

exposing the semiconductor substrate on one or more areas proximal to the gate electrode **312 & 310 (column 6, lines 19-37, Please see details in the manufacturing method H )**;

providing for a thin film of metal on at least a portion of the exposed semiconductor substrate **300 (column 6, line 33)**;

and reacting the metal with the exposed semiconductor substrate such that a Schottky or Schottky-like source electrode and drain electrode are formed on the semiconductor substrate **(column 6, lines 19-37, Please see details in the manufacturing method H )**.

50. With respect to claim 56, Matsuo discloses the method of claim 55, wherein the gate electrode is provided by:

depositing a thin conducting film **311** on the insulating layer **309, 313, & 314**;

patterning and etching the conducting film **311** to form a gate electrode **312 & 310** ;

and forming one or more thin insulating layers **309 & 314** on one or more sidewalls of the gate electrode .

51. With respect to claim 57, Matsuo discloses the method of claim 55, further comprising removing metal not reacted during the reacting process (**column 6, lines 37-39 see more details in the manufacturing method H**).

52. With respect to claim 58, Matsuo discloses the method of claim 55, wherein the reacting comprises thermal annealing (**column 6, lines 35, see more details in the manufacturing method H**).

53. With respect to claim 60, Matsuo discloses the method of claim 55, wherein the source and drain electrodes are formed from a member of the group consisting of the rare earth silicides (**column 11, lines 25-40, please note yttrium and cerium are rare earth materials**).

54. With respect to 61, Matsuo the method of claim 55, wherein the insulating layer is formed from a member of the group consisting of metal oxides **313 & 314 (column 34, lines 25-27)**.

55. With respect to claim 62, Matsuo discloses the method of claim 55, wherein the insulating layer **313, & 314** is formed from an oxy-nitride stack **314 (Column 10, lines 52-67 & column 11, lines 1-30)**.

56. With respect to claim 63, Matsuo discloses the method of claim 55, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel **(column 6, lines 19-59, see more details in the manufacturing method H)**.

57. With respect to claim 64, Matsuo discloses the method of claim 55, wherein an entire interface between at least one of the source electrode and the drain electrode **305, 307, & 317** and the semiconductor substrate **300** forms a Schottky contact or Schottky-like region with the semiconductor substrate **(column 6, lines 19-59, see more details in the manufacturing method H)**.

58. With respect to claim 65, Matsuo discloses the method of claim 55, wherein dopants **305** are introduced into the channel region.

Art Unit: 2823

59. Claims 2, 16, 25, 37, 48, & 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo et al (US6737716 B1) in view of Morris et al (US 5,140,383).

60. With respect to claims 2, Matsuo discloses, the method of claim 1, where in the source and drain electrodes **305, 307, & 317** are formed from Platinum silicide and palladium silicide (**column 32, lines 27-33**).

However, Matsuo fails to teach, the method of claim 1, wherein the source and drain electrodes are formed from a member of the group consisting of: iridium silicide.

Morris teaches the method of claim 1, wherein the source and drain electrodes are formed from a member of the group consisting of: iridium silicide (column 1, lines 60-62).

Matsuo and Morris are analogous art because they are from the same field of endeavor and method of forming Schottky contact on semiconductor device.

At the time of invention it would have been obvious to one of ordinary skill in the art to incorporate the element of Morris in view of Matsuo in a method for manufacturing of semiconductor process because of "a higher Schottky diode characteristic than aluminum, a typical contact metal" (column 1, lines 52-53).

Art Unit: 2823

Therefore, it would have been obvious to combine Morris with Matsuo for the benefit of a higher Schottky diode characteristic contact to obtain the invention as specified in claim 2.

61. Claims 16, 25, 37, 48, & 59 are rejected because of the reasons above.

62. Claims 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuo (US6737716 B1).

63. With respect to claims 10, 11 & 13 Matsuo teaches claims 10, 11 & 13. Since claims 10, 11 & 13 are dependent upon claim 2, those claims are rejected under U.S.C. 103(a).

With respect to claim 10, the method of claim 2 or 3, wherein the insulating layer is formed from a member of the group consisting of metal oxides **313 & 314 (column 34, lines 25-27)**.

With respect to claim 11, the method of claim 2 or 3, wherein the insulating layer is formed from an oxy-nitride stack **314 (Column 10, lines 52-67 & column 11, lines 1-30)**.

With respect claim13, the method of claim 11, wherein the Schottky contact or Schottky-like region is formed at least in areas adjacent to the channel, and wherein dopants are introduced into the channel region (**column 6, lines 19-59, see more details in the manufacturing method H**).

64. With respect claim14, the method of claim 2 or 3, wherein providing a source electrode and a drain electrode in contact with the semiconductor substrate is performed at a processing temperature of less than about 800 °C.

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. *See In re Aller, Lacey and Hall* (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodru* ; 919 f 2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)

Art Unit: 2823

Appellants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. *Ex parte Ishizake*, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. *In re Burckel*, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

### ***Conclusion***

65. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The Calviello (US 4,312,113) reference respectively teaches a method of fabricating semiconductor with high dielectric constant insulators.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Su C. Kim whose telephone number is (571) 272-5972. The examiner can normally be reached on Monday - Friday, 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaudhuri Olik can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'W. David Coleman', with a stylized, flowing script.

**W. DAVID COLEMAN  
PRIMARY EXAMINER**